REMARKS

Claims 1-3, 8-15, 18, 38, 40-45 and 50-53 are pending in the application. In the Office Action dated February 11, 2003, the Examiner rejected claims 1-3, 8-15, 18, 38 and 40-45 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,169,328 to Mitchell ("Mitchell") in view of U.S. Patent No. 5,461,255 to Chan *et al.* ("Chan"). The Examiner further rejected claims 50-53 under 35 U.S.C. § 103(a) as being unpatentable over Mitchell in view of Chan as applied to claims 1-3, 8-15, 18, 38 and 40-45 above, and further in view of U.S. Patent No. 5,461,087 to Takahashi *et al.* ("Takahashi"). Applicant respectfully requests reconsideration of the application in view of the foregoing amendments and the following remarks.

The disclosed embodiments of the application will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, as well as the discussion of the differences between the disclosed embodiments and the prior art subject matter are not to be construed to define the scope or interpretation of any of the claims. Instead, such discussed differences are offered merely to help the Examiner appreciate important claim distinctions as they are discussed.

The various embodiments of the present invention are directed to a semiconductor package assembly having a plurality of relatively thin strips of a compliant adhesive film to adhere a semiconductor die to a substrate or interposer. The compliant adhesive film is interposed between the semiconductor die and the interposer and is generally segmented into a plurality of elongated strips having relatively narrow widths. The compliant adhesive film is positioned between the die and the interposer to reduce undesired shear stresses that may result from unmatched coefficients of thermal expansion for the interposer and the semiconductor die. As a result, failures in semiconductor package interconnections, such as solder bonds, or other interconnections are advantageously reduced.

Referring to Figures 3A and 3B in the present application, and to the corresponding description on pages 8 and 9, a further advantage afforded by the various embodiments is that the cumulative thermal expansion for the multiple, relatively narrow strips of adhesive film, as shown in detail in Figure 3A is significantly lower than the thermal expansion for one or more relatively wide layers of an elastomeric film, as shown in the prior art device in Figure 3B. As a consequence, the aforementioned thermal stress on the package wire

bond joints resulting from the different coefficients of thermal expansion between the die and the substrate are significantly reduced. Thus, the use of the relatively narrow strips of adhesive film has significant thermal stress reduction advantages over one or more relatively wide strips of material.

The Examiner has cited the Mitchell reference for disclosing a semiconductor chip package that includes a semiconductor chip and a printed wire board (PWB) spaced apart from the semiconductor chip. Positioned between the chip and the PWB is a plurality of elastic compliant pads forming columnar supports for the chip. Referring first to Figure 1, the elastic compliant pads 110 are clearly shown. The compliant pads 110 are made of a curable liquid elastomer, such a silicone elastomer (col. 5, lines 2-6). The pads are arranged in a grid pattern (col. 5, lines 15-18) using a stencil mask (col. 5, lines 25-30). The Examiner has further referred to Figure 4B of Mitchell as depicting an elongated adhesive pad 110 positioned between the semiconductor chip and the PWB. However, the applicant notes that the pad 110 is comprised of the curable liquid elastomer referred to earlier, and fails entirely to disclose elongated strips of a compliant adhesive film that include a compliant carrier layer that has a pair of opposing surfaces with adhesive layers disposed on the surfaces.

The Examiner has also cited the Chan reference for disclosing a semiconductor package that includes a multiplayer conductive lead frame assembly attached to a chip with adhesive strips. Specifically, Chan is directed to a semiconductor package that provides improved *electrical isolation* of signal lines and power and bus lines that are coupled to the chip. (col. 3, lines 10-15). With reference now to Figure 3 of Chan, a semiconductor package 10 according to the invention is shown. A main lead frame 22 extends across a semiconductor circuit chip 12 to connect to a plurality of bond pads 18 that are arranged along a bisecting axis 14 of the semiconductor circuit chip 12. In order to securely attach the lead frame 22 to the semiconductor circuit chip 12, dual-sided adhesive tape strips 20 are positioned between the lead frame 22 and the circuit chip 12. The strips 20 are *relatively wide strips* to provide for secure attachment of the lead frame 22 to the circuit chip 12. In fact, the strips 20 shown in Figure 3 collectively extend across substantially the entire width of the circuit chip 12, and leave only a slight gap between the strips 20 so that the lead frame 22 may be attached to the chip 12 at the

bond pads 18. Accordingly, Chan teaches the use of relatively wide adhesive strips in order to provide the required mechanical adhesion between the lead frame 22 and the chip 12.

Still referring to Figure 3, a bus lead frame 30 is positioned on the lead frame 22, and is separated from the lead frame 22 by a pair of adhesive tape strips 28. Although the strips 28 are slightly narrower that the broad strips 20, the function of the strips is to provide a secure mechanical connection between the bus frame 30 and the lead frame 22. Of equal importance is the requirement that the strips 28 provide enhanced levels of electrical isolation between the lead frame 22 and the bus lead frame 30, since, as stated in the background section of Chan reference, a particular problem associated with semiconductor packages of the type shown is electrical shorting of the bus lines to signal lines.

As a result, the Chan reference teaches the advantages associated with the use of wide strips of adhesive material, so that secure mechanical connection between lead frames and the chip are attained, and to further provide for enhanced electrical isolation between adjacent lead frame assemblies. These requirements are, however, simply not compatible with the use of narrow strips of adhesive material positioned between an interposer and a semiconductor die, as disclosed in the present application. Specifically, this issue was fully addressed in pages 8 and 9 of the present application, as discussed more fully above. Moreover, referring again to Figures 3A and 3A in the present application, the prior art device shown in detail in Figure 3B has a relatively wide strip of an adhesive material that was conclusively shown to provide inferior thermal stress mismatch properties when compared to the relatively narrow adhesive strips shown in Figure 3A. Accordingly, applicants respectfully assert that the Chan reference *teaches away* from the embodiments of the present invention by teaching the use of relatively wide strips of adhesive material.

Further, the undersigned cannot find any relevant teaching that describes the use of narrow strips of adhesive material to minimize thermal mismatch problems between a semiconductor die and an interposer. In fact, the undersigned cannot find *any reference* in Chan to the thermal mismatch difficulties discussed in detail in the present application, much less *any teaching* that suggests that the package disclosed by Chan may be used to reduce thermal mismatch problems in semiconductor packages. If the undersigned has missed a relevant

teaching in the Chan reference, the Examiner is requested to contact the undersigned attorney to particularly point out where this pertinent reference may be found.

The Examiner has also cited the Takahashi reference for disclosing an adhesive composition that is curable upon exposure to ultraviolet light, and more particularly, a double-sided adhesive tape that includes a pair of porous base sheets that may be impregnated with the disclosed adhesive material during the curing process.

Turning now to the claims, patentable differences between the claims and the applied art will be specifically pointed out. Claim 1, as amended, recites in pertinent part, "A semiconductor device package, comprising...a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges and disposed between the semiconductor die and the interposer, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges of the semiconductor die*, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, *the plurality of adhesive film strips being operable to reduce a thermal mismatch stress between the semiconductor die and the interposer.*" (Emphasis added). As discussed more fully above, Mitchell does not disclose strips having a compliant carrier layer. Instead, Mitchell discloses elastomeric posts that extend between a die and an interposer. The Chan reference further fails to disclose or suggest in any motivated sense, the use of strips of relatively narrow width such that the sum of the widths is *substantially less* than a width of the package. Accordingly, claim 1 is allowable over the cited combination. Further, claims that depend from claim 1 are also allowable based upon the allowability of the base claim and further in view of the additional limitations in these claims.

Claim 11 as amended recites in pertinent part, "A device package assembly for a semiconductor die being constructed from a process comprising...attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one

electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges, the strips of compliant adhesive film having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges*, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, *the plurality of adhesive film strips being further operable to reduce a thermal mismatch stress between the semiconductor die and the interposer....*" (Emphasis added). Again, Mitchell does not disclose this. Further, the Chan reference does not disclose that the strips have respective widths such that a sum of the widths is substantially less than a width of the interposer. Instead, Chan discloses adhesive strips that extend *substantially the entire width* of a semiconductor device to which the strips are applied. Accordingly, claim 11 is also allowable over the cited art. Claims depending from claim 11 are similarly allowable based upon the allowability of the base claim and further in view of the additional limitations recited in the dependent claims.

Claim 38 as amended recites in pertinent part, "A semiconductor device package, comprising...a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges*, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, *the plurality of adhesive film strips being operable to reduce a thermal mismatch stress between the semiconductor die and the*

interposer." (Emphasis added). As described in greater detail above, the Mitchell reference does not disclose adhesive strips having a compliant layer. Mitchell discloses, at most, short columnar elastomeric structures that extend between a semiconductor die and an interposer. Chan discloses adhesive strips, but does not disclose adhesive strips that extend across a portion of a width of the first surface, such that a sum of the widths of the strips is substantially less than the width of the first surface. Instead, Chan discloses wide strips suited to mount leadframe structures, that extend substantially the entire width of a semiconductor substrate. Claim 38 is therefore allowable over the cited art. Further, claims depending from claim 14 are also allowable based on the allowable form of the base claim and further in view of the additional limitations recited in the dependent claims.

Finally, claim 42 as amended recites in pertinent part, "A semiconductor device package, comprising...a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die to adhere the semiconductor die to the die attach surface of the interposer, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges*, the strips of compliant adhesive film further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, *the plurality of adhesive film strips being operable to reduce a thermal mismatch stress between the semiconductor die and the interposer.*" (Emphasis added). Yet again, the Mitchell and Chan references, either singly or in combination, fail to disclose this. Accordingly, claim 42 is allowable. Claims depending from claim 42 are similarly allowable based upon the allowability of the base claim and further in view of the additional limitations recited in the dependent claims.

Applicant respectfully submits that the foregoing amendments also fully address the claim rejections based on the Takahashi reference, since these rejections stemmed from the combination of the Mitchell and Chan references.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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